AMENDMENTS TO THE CLAIMS

Claims 1-64. (Canceled)

65. (Previously presented) A method of forming an MIS capacitor on a semiconductor substrate, comprising the acts of:

forming a semiconductive layer of hemispherical grained polysilicon over a substrate;

opening the grains which form said layer of hemispherical grained polysilicon to activate said grains;

forming a dielectric layer comprising aluminum oxide over said semiconductive layer by atomic layer deposition; and

forming a metal nitride layer over said dielectric layer.

66. (Canceled)

67. (Canceled)

68. (Previously presented) The method of claim 65, wherein said act of opening said grains further comprising etching said layer of hemispherical grained polysilicon to form an etched layer of hemispherical grained polysilicon.

69. (Previously presented) The method of claim 68, wherein said act of etching said layer of hemispherical grained polysilicon further comprises contacting said layer of hemispherical grained polysilicon with a solution of HF.

70. (Original) The method of claim 69 further comprising the act of subjecting said layer of hemispherical grained polysilicon to an RTN process.

71. (Original) The method of claim 69 further comprising the act of subjecting said layer of hemispherical grained polysilicon to an anneal process.

72. (Original) The method of claim 69 further comprising the act of subjecting said layer of hemispherical grained polysilicon to a PH_3 anneal.

73. (Original) The method of claim 65, wherein said metal nitride layer is a titanium nitride layer formed by CVD.

74. (Original) The method of claim 65, wherein said metal nitride layer is a titanium nitride layer formed by ALD.

75. (Original) The method of claim 74, wherein said titanium nitride layer is formed by ALD using a nitrogen source and a titanium source precursor.

76. (Currently amended) ~~The method of claim 65,~~ A method of forming an MIS capacitor on a semiconductor substrate, comprising the acts of:

forming a semiconductive layer of hemispherical grained polysilicon over a substrate;

opening the grains which form said layer of hemispherical grained polysilicon to activate said grains;

forming a dielectric layer comprising aluminum oxide over said semiconductive layer by atomic layer deposition; and

forming a metal nitride layer over said dielectric layer, wherein said metal nitride layer is a boron-doped titanium nitride layer formed by CVD.

77. (Previously presented) The method of claim 76, wherein said act of providing said boron-doped titanium nitride layer further comprises the act of incorporating boron into a titanium nitride layer.

78. (Currently amended) The method of claim ~~78~~ 77, wherein said act of incorporating boron into a titanium nitride layer further comprises the act of exposing said titanium nitride layer to B_2H_6.

79. (Currently amended) The method of claim ~~79~~ 78, wherein said act of incorporating boron into a titanium nitride layer further comprises the act of exposing said titanium nitride layer to B_2H_6 at a temperature of about 200°C to about 600°C.

80. (Original) The method of claim 65, wherein said metal nitride layer is a tungsten nitride layer formed by CVD.

81. (Original) The method of claim 65, wherein said metal nitride layer is a tungsten nitride layer formed by ALD.

82. (Original) The method of claim 65, wherein said metal nitride layer is a boron-doped tungsten nitride layer formed by CVD.

83. (Original) The method of claim 82, wherein said act of providing said boron-doped tungsten nitride layer further comprises the act of incorporating boron into a tungsten nitride layer.

84. (Original) The method of claim 65, wherein said aluminum oxide dielectric layer is formed by ALD using an ozone source and an aluminum source precursor.

85. (Previously presented) The method of claim 84, wherein said aluminum source precursor is trimethyl-aluminum.

86. (Original) The method of claim 65, wherein said aluminum oxide dielectric layer is formed to a thickness of about 10 Angstroms to about 500 Angstroms.

87. (Original) The method of claim 86, wherein said aluminum oxide dielectric layer is formed to a thickness of about 25 Angstroms to about 100 Angstroms.

88. (Original) The method of claim 65, wherein said aluminum oxide dielectric layer further comprises a material selected from the group consisting of tantalum oxide, zirconium oxide, hafnium oxide, hafnium-aluminum-oxygen alloys and lanthanum-aluminum-oxygen alloys.

89. (Original) The method of claim 88, wherein said aluminum oxide dielectric layer is formed as a composite stack of at least one aluminum oxide layer and at least one tantalum oxide layer.

90. (Original) The method of claim 89, wherein said aluminum oxide dielectric layer is formed of interleaved layers of aluminum oxide and tantalum oxide.

91. (Original) The method of claim 90, wherein said aluminum oxide dielectric layer is an aluminum oxide /tantalum oxide /aluminum oxide stack.

92. (Original) A method of forming an aluminum oxide MIS capacitor on a semiconductor substrate, comprising the acts of:

forming a lower capacitor electrode of hemispherical grained polysilicon over said semiconductor substrate;

forming a dielectric composite stack comprising aluminum oxide over said lower capacitor electrode; and

forming an upper capacitor electrode of tungsten nitride over said dielectric composite stack.

93. (Original) The method of claim 92, wherein said dielectric composite stack is formed by ALD.

94. (Original) The method of claim 93, wherein said dielectric composite stack is formed of interleaved layers of aluminum oxide and another metal oxide material.

95. (Original) The method of claim 94, wherein said metal oxide material is selected from the group consisting of tantalum oxide, zirconium oxide, hafnium oxide, hafnium-aluminum-oxygen alloys and lanthanum-aluminum-oxygen alloys.

96. (Original) The method of claim 92 further comprising the act of subjecting said dielectric composite stack to a nitridizing treatment.

97. (Original) The method of claim 96 further comprising the act of subjecting said dielectric composite stack to a PH_3 anneal treatment.

98. (Original) The method of claim 92, wherein said tungsten nitride layer is formed by ALD using a tungsten source and a nitrogen source precursor.

99. (Original) The method of claim 92 further comprising the act of etching said hemispherical grained polysilicon to form an etched hemispherical grained polysilicon.

100. (Original) The method of claim 99, wherein said act of etching said hemispherical grained polysilicon further comprises contacting said hemispherical grained polysilicon with a solution of HF.

101. (Original) The method of claim 100 further comprising the act of subjecting said hemispherical grained polysilicon to a PH_3 anneal.

102. (Original) The method of claim 101 further comprising the act of subjecting said hemispherical grained polysilicon to an RTN treatment.

103. (Original) The method of claim 102 further comprising the act of subjecting said hemispherical grained polysilicon to a HF solution after said PH_3 anneal and before said RTN treatment.